



21st IEEE International conference on
Design, Test & Technology of Integrated Systems
November 4 - 6, 2026, Hammamet, Tunisia



Call for Participation for Special session Emerging Memory AI Accelerator Test and Reliability



It is our pleasure to invite you to participate in the IEEE International Conference on Design, Test and Technology of Integrated Systems (DTTIS 2026).

DTTIS'26 is organized by National Engineer School of Sfax in collaboration with the IEEE Tunisia section and co-sponsored by the IEEE Computer society TTTC. The event is going to be organized on November 4 - 6, 2026.

IEEE DTTIS'26 represents a scientific and technological event dedicated to integrated electronic systems which reach the nanoscale era. The interests of the conference cover all the aspects from the design to the test of micro and nano systems. IEEE DTTIS'26 is an important meeting where well-known researchers from universities and companies will present the latest innovations in the field of micro and nano electronics.

It will also provide engineers with an opportunity to interact and share their experiences in industry and technology applications.

Special Session Topics :

Emerging memories and memristor-based architectures are becoming promising solutions for next-generation artificial intelligence accelerators due to their high performance, low power consumption, and efficient implementation of vector-matrix operations. However, these technologies introduce significant challenges related to testing, defects, aging, and hardware reliability. As AI accelerators become increasingly integrated into advanced computing systems, ensuring their robustness and reliability has become a critical research issue. This special session focuses on the test and reliability aspects of emerging memory-based AI accelerators, highlighting defect mechanisms, fault modeling, aging effects, and efficient test strategies for both manufacturing and in-field operation.

The scope of this special session includes, but is not limited to the following topics:

- Memristor-based AI accelerators
- Test strategies for emerging memory circuits
- Fault modeling and defect analysis in AI hardware
- Reliability challenges in emerging memories
- Aging effects in AI accelerator architectures
- Hardware reliability solutions for AI systems
- In-field and post-manufacturing testing techniques
- Emerging memory technologies for neural network accelerators

The conference paper should be prepared according to the IEEE standard format. The manuscript should be written in English using a two-column layout on A4 or Letter-size paper. Authors are required to use the official IEEE conference template available in Microsoft Word or LaTeX formats.

IEEE Templates : <https://www.ieee.org/conferences/publishing/templates>

Papers should be sent to one of the two organizers:



Dr. Hassen Aziza

Aix Marseille University, France
hassen.aziza@univ-amu.fr



Dr. Moritz Fieback

Delft University of Technology, NL
M.C.R.Fieback@tudelft.nl

